REMARKS

Claims 1-20 are pending in the application.

Claims 1-8 and 19 stand withdrawn as non-elected and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 9-18 and 20 are rejected.

No new matter is added.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Rejections-35 USC § 103

Claims 9-18, 20, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art, and in view of U.S. Patent No. 6,232,179, Sato ("Sato"). Applicant respectfully traverses the rejection.

The Examiner cites Applicant Admitted Prior Art (AAPA) as disclosing a method of forming a non-volatile memory device that has all the elements of claim 9 and 20, except that AAPA fails to disclose the step of forming a second gate spacer on the first spacers to fill the first spacer, the second gate spacers comprising an insulating material having a relatively high dielectric constant. The Examiner further cites Sato as disclosing a method of forming gate electrodes comprising the steps of forming first spacers 14 (Fig. 4) wherein the first spacer comprises a relatively low dielectric constant, and forming second spacers on the first spacers wherein the second spacers 15 (Fig. 4) comprises an insulating material having a relatively high dielectric constant.

On the contrary, as shown in the figures of Sato, second spacers (element 15 in Figs. 1, 2, and 4; element 28 in Figs. 5, 6, and 7; element 56 in Figs. 8 and 9) overlay first spacers (element 14 in Figs. 1, 2, and 4; element 27 in Figs. 5, 6, and 7; element 55 in Figs. 8 and 9).

Although claims 9 and 20 cite second spacers on the first spacers, claims 9 and 20 also cite that the second spacers are formed on the first spacers *to fill the first space.* Sato does not disclose this construction, in fact Sato teaches away from filling in the space between gate stack structures comprised of elements 22-24 (Fig. 6B – Fig. 7B). In particular, Sato shows how the open space between the gate stack structures in necessary to carry out the etching process of layer 21X in Fig. 6B (also see text col. 11, lines 15-20). For at least this reason, the rejection does not present a prima facie case of obviousness. Therefore, claims 9 and 20 are not obvious over AAPA in view of Sato, and are both in allowable condition.

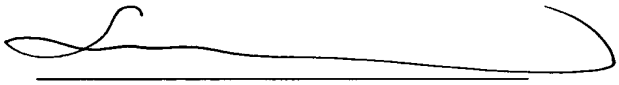
In addition, claims 10 – 18, which contain all the elements and features of base claim 9, are also in condition of allowance, for their dependency and their own merits.

For the foregoing reasons, reconsideration and allowance of claims 9-18, and 20 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Hosoon Lee
Limited Recognition Under 37 CFR § 10.9(b)

MARGER JOHNSON & McCOLLOM, P.C.
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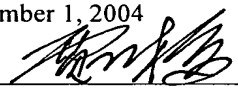
Portland, OR 97205
503-222-3613

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment Commissioner for Patents, Washington, DC 20231
Date: December 1, 2004



Li Mei Vermilya

IN THE DRAWINGS

Please replace FIGS. 1A-4F with the enclosed revised FIGS. 1A-4F, in which the word "PERIPHERIAL" is replaced with the correct word "PERIPHERAL."

FIG. 1A
(PRIOR ART)

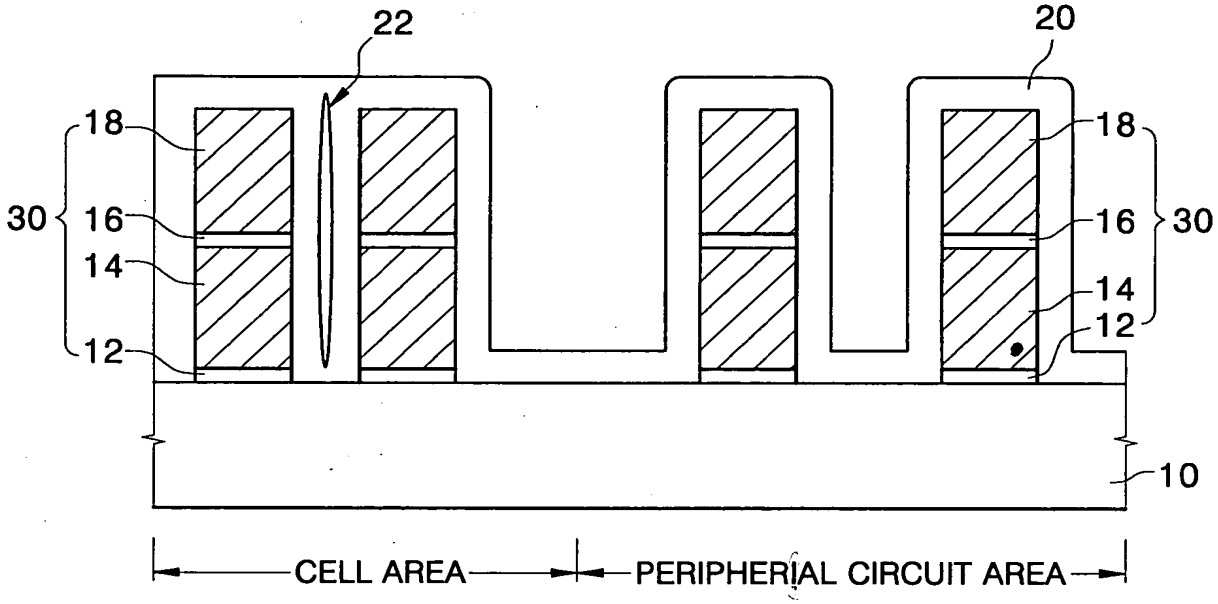


FIG. 1B
(PRIOR ART)

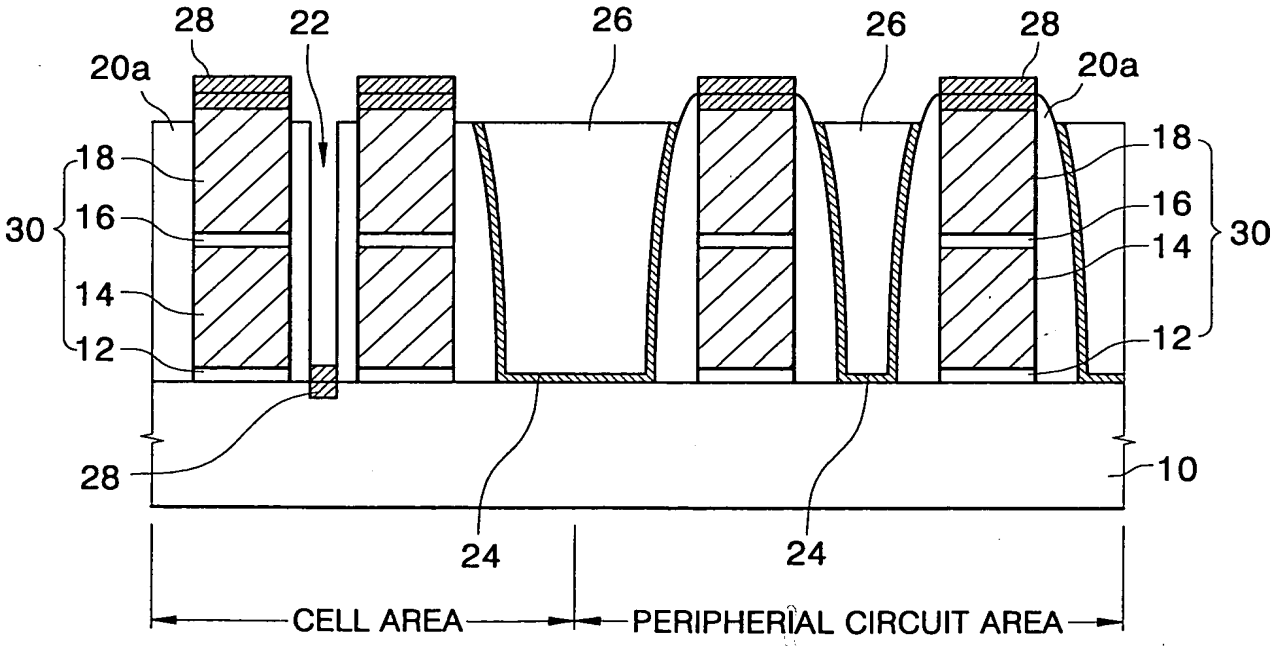


FIG. 2

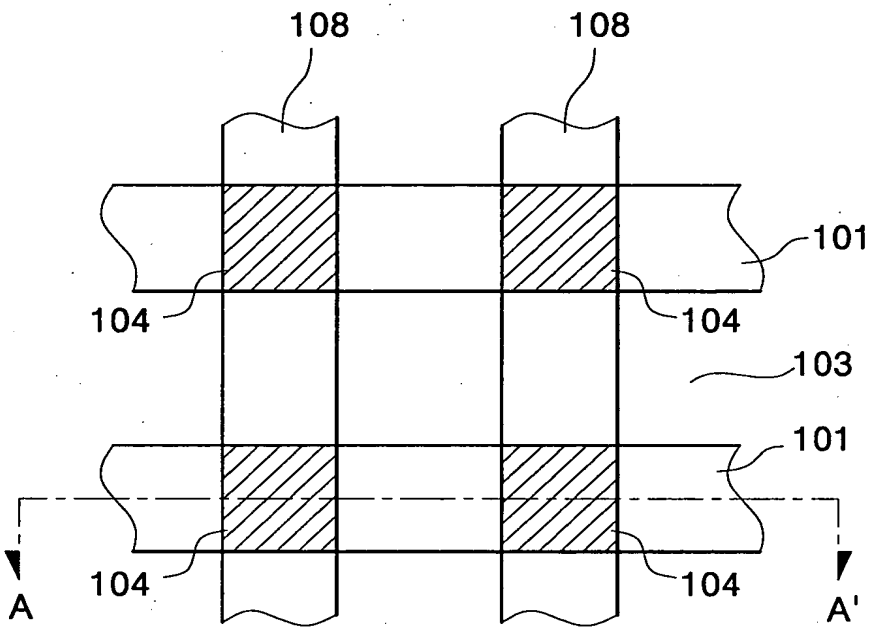
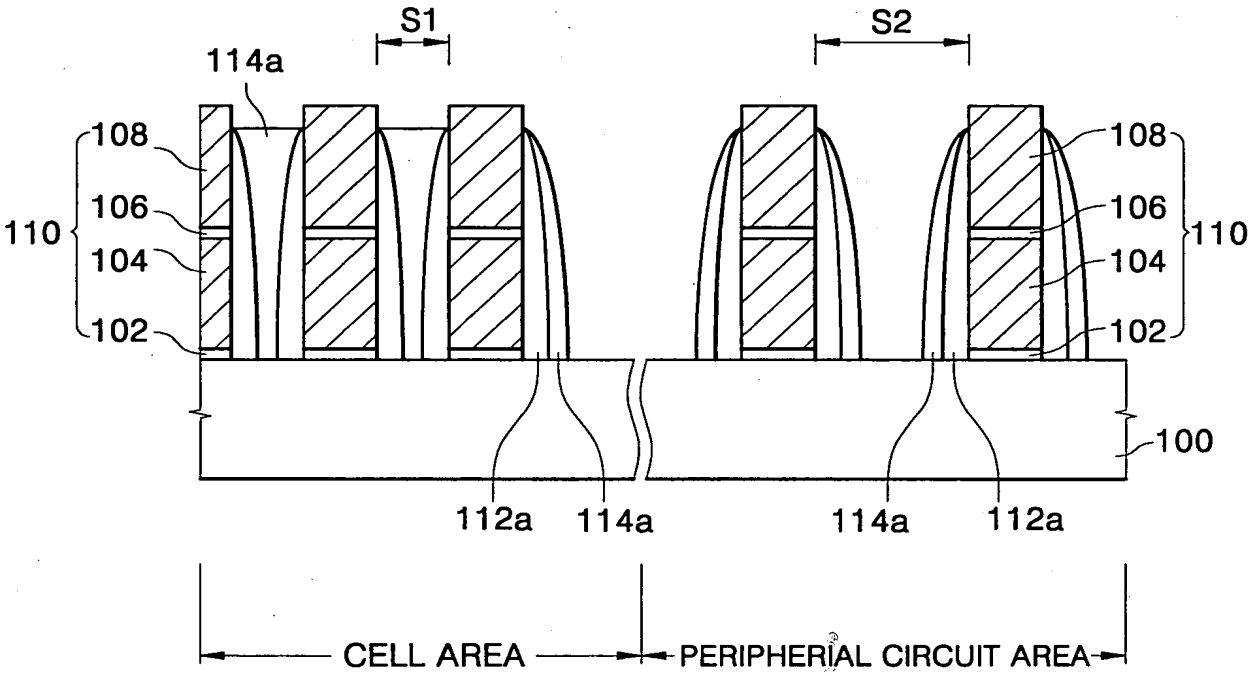


FIG. 3


S1
S2
114a
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106
104
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112a
114a
114a
112a
CELL AREA
PERIPHERIAL CIRCUIT AREA

FIG. 4A

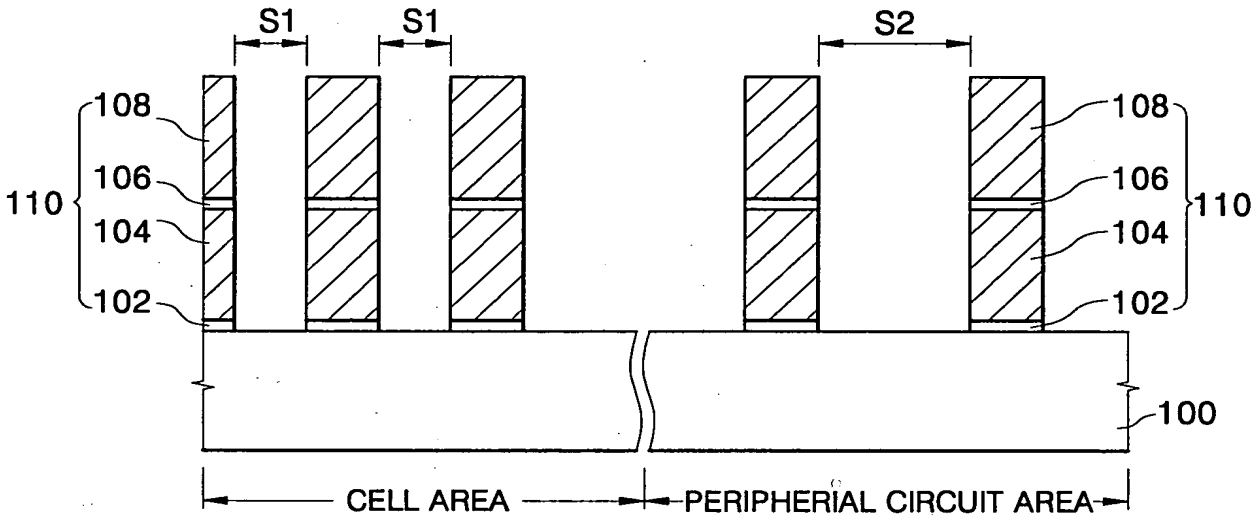
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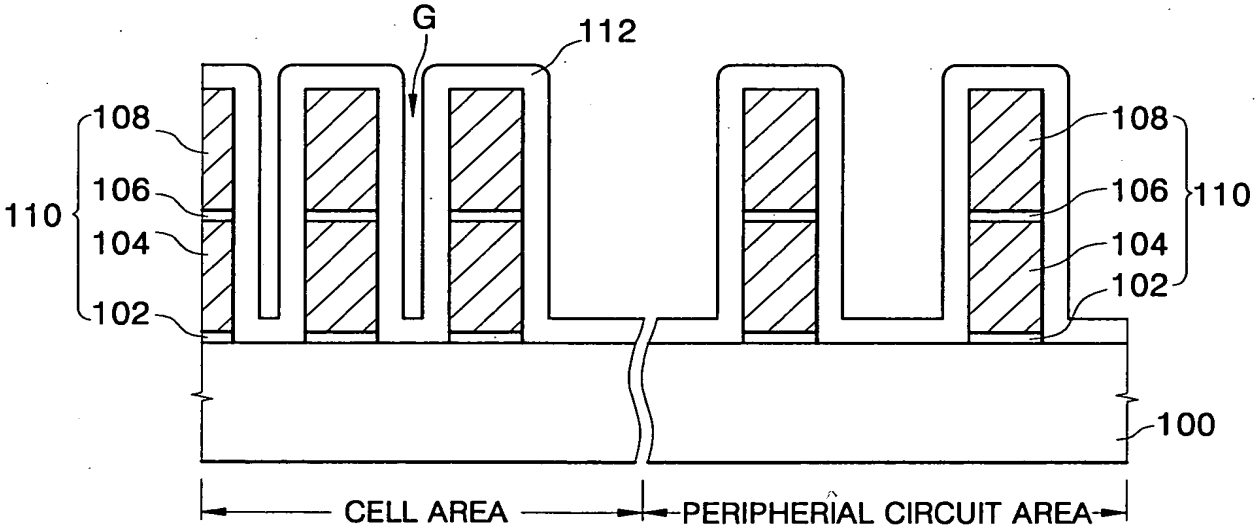
FIG. 4B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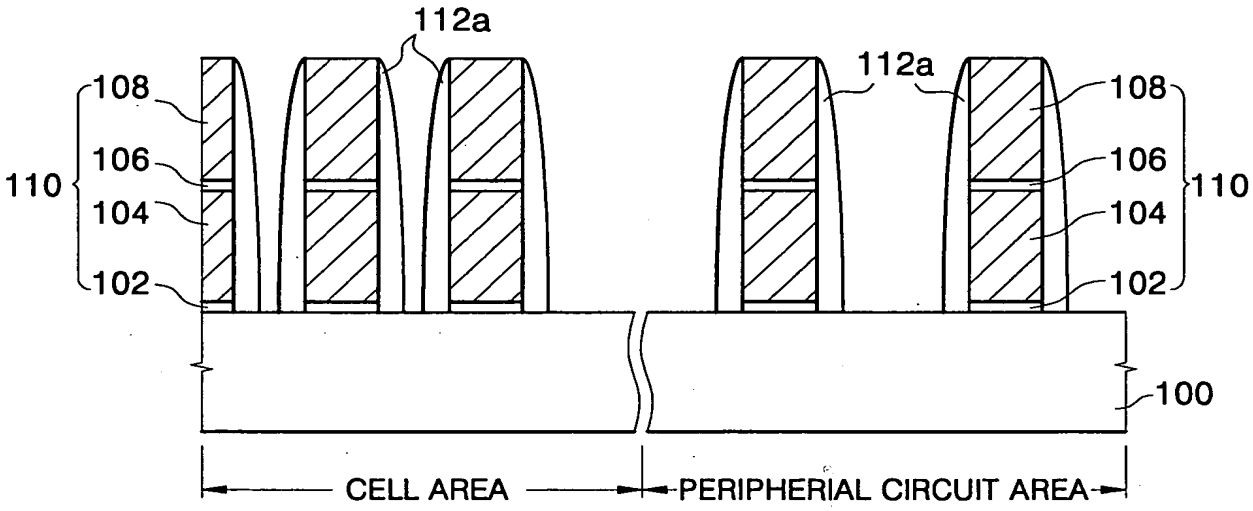
CELL AREA
PERIPHERIAL CIRCUIT AREA

FIG. 4C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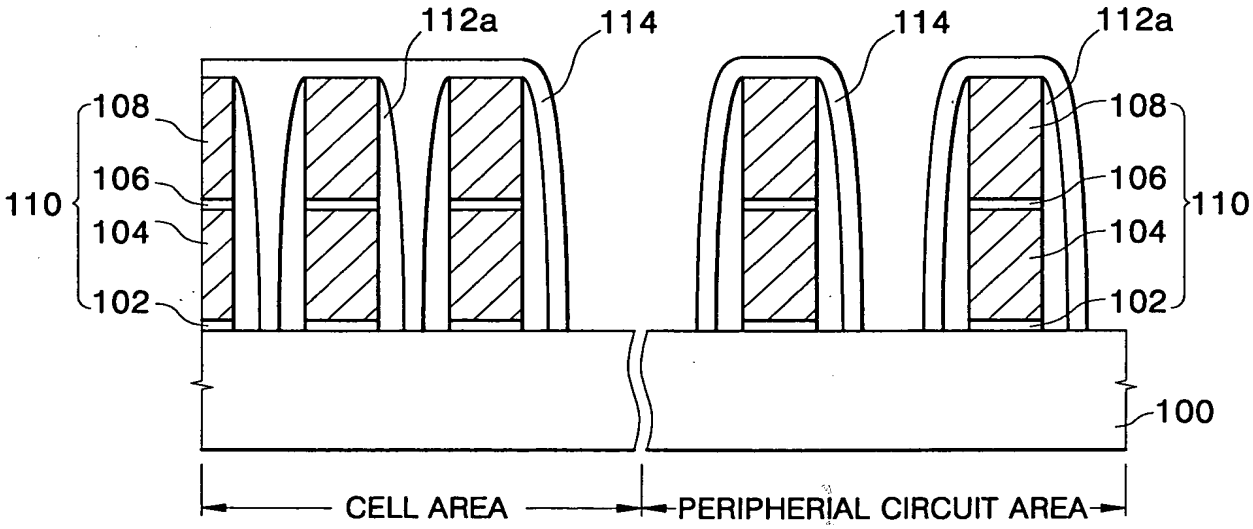
CELL AREA
PERIPHERIAL CIRCUIT AREA

FIG. 4D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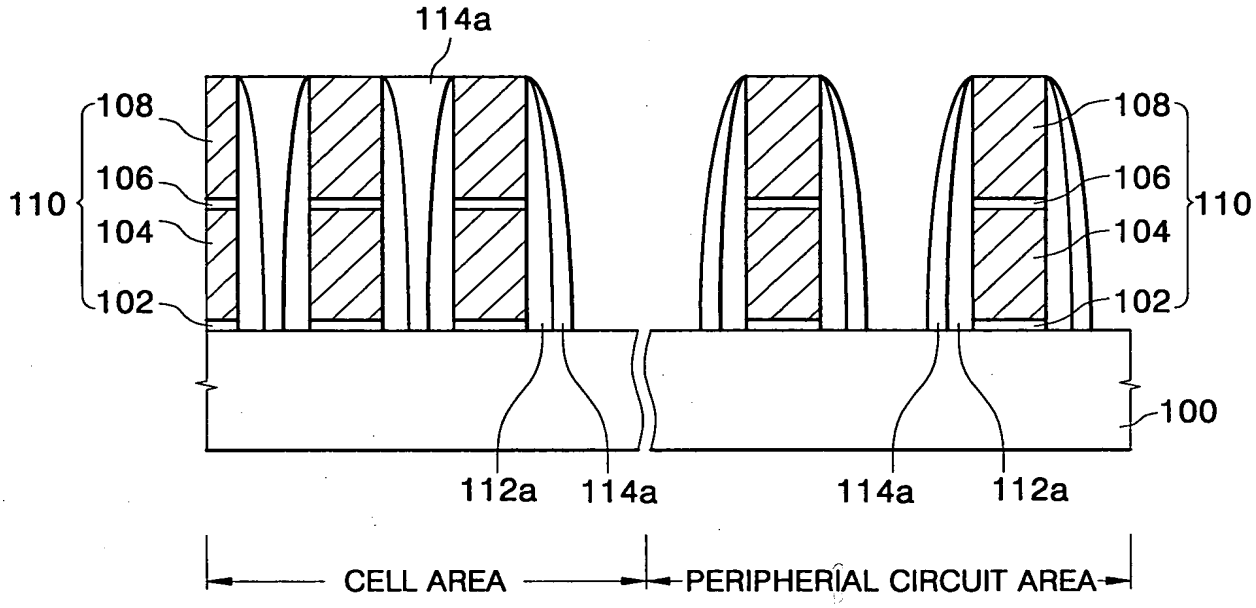
CELL AREA
PERIPHERIAL CIRCUIT AREA

FIG. 4E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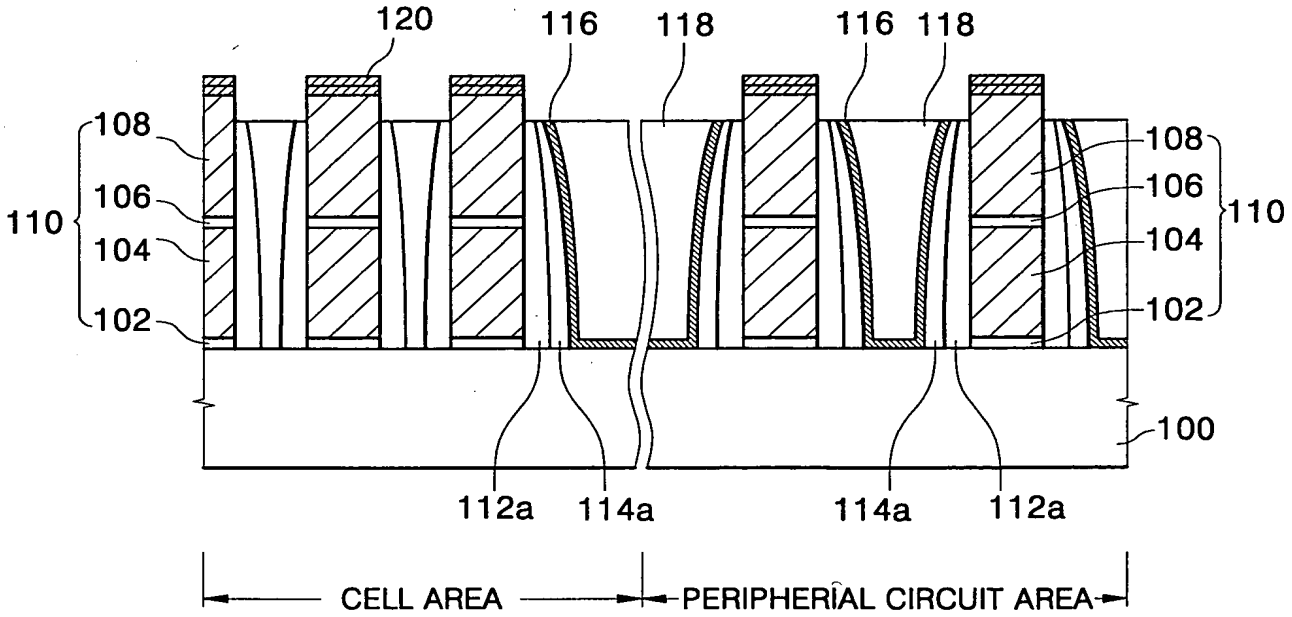
CELL AREA
PERIPHERIAL CIRCUIT AREA

FIG. 4F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114a
112a
CELL AREA
PERIPHERIAL CIRCUIT AREA